Claims

1. Method for simulation of an electronic circuit, the circuit being represented by a network of a plurality of logic elements, the circuit comprising first and second asynchronous clock domains, whereby jitter elements are additionally inserted at predetermined portions of circuit boundaries between the first and second clock domains, the jitter elements being represented as logic elements, the values of which are randomly set.

2. The method of claim 1, wherein the simulation is carried out on cycle level of a description of the electronic circuit.

3. The method of claim 1, wherein the jitter elements comprise delay elements for introducing predetermined timing delays which are randomly exercised.

4. The method of claim 1, wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

5. The method of claim 3, wherein the jitter elements are interactively inserted by a user.

6. The method of claim 3, wherein the jitter elements are automatically inserted using predetermined modules.

7. Method of designing an electronic circuit, comprising a step of simulating the electronic circuit according to claim 1.

8. Simulation system for simulation of an electronic circuit, the circuit being representable by a network of logical elements, the circuit comprising first and second asynchronous clock domains, wherein jitter elements are additionally insertable at predetermined portions of circuit boundaries between the first and second clock domains, the jitter elements being representable as logical elements, the values of which are randomly set.

9. The system of claim 8, wherein the simulation is carried out on cycle level of a description of the electronic circuit.

10. The system of claim 8, wherein the jitter elements comprise delay elements for introducing predetermined timing delays which is randomly exercised.

11. The system of claim 8, wherein the jitter elements comprise x generator elements for introducing predetermined signal values which are randomly generated.

12. The system of claim 8, wherein the jitter elements are interactively inserted by a user.

13. The system of claim 8, wherein the jitter elements are automatically inserted using predetermined modules.

14. A computer-readable storage medium comprising program code for performing the method according to claim 1, when loaded into a computer system.

15. A computer-readable storage medium comprising program code for performing the method according to claim 7, when loaded into a computer system.